EE/CprE/SE 491 WEEKLY REPORT 07
Nov 5 – Nov 11

Group number: **22**

Project title: **ReRAM Compute Asic Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**
  - This week, we continued working with basic modules in the open-source tools, along with discussing some of the base tests that need to be able to run no matter what (forming, setting, and resetting of reram cells), along with some other additions to measurements that we might want to take during the tests we've already discussed. We also explored some other basic modules to consider such as a new basic selector circuit that supposedly works better than the standard 1T1R.

- **Past week accomplishments**
  - Vinicius Malaman Soares: Tried to fix last week's error, did not work out. Got the tools setup on a VM, completed inverter simulation on the new setup, but ReRAM runs into an error when simulating now. I have been working on fixing this error since it appeared.
  - Tyler Kloser: Decompose characteristic designs and design specific quantization for primary goals
  - Ali Mannan: Continued work on laying out ReRAM, and ran some preliminary simulations on the ReRAM based on the characterizations laid out by Austin and approved by the client.
  - Austin Miller: Compiled test modules and basic diagrams for some of the Primary Goal modules we will likely implement with some explanation of how they cater to our test/measurement goals
- **Pending issues**
  - Tyler Kloser: N/A
  - Ali Mannan: N/A
  - Austin Miller: Need to figure out how many physical pins we can/should use
  - Vinicius Malaman Soares: Figure out why the ReRAM is not simulating.

- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Tyler Kloser	Understanding design characteristics and look into some of the new suggestions from client	6	43
Ali Mannan	Running characterizations based off the simulation	5	52
Austin Miller	Explored test structures/modules. Found a new option for basic cell (1T1R), now (1D1T1R), exploring the viability of it as an option for testing	6	51 (not updated)
Vinicius Malaman Soares	Got a new VM and set it up with the tools and pdk, simulated basic circuits.	6	48

- **Comments and extended discussion**
  - N/A

Plans for the upcoming week

- Ali Mannan: Bring into schematic the new structures for ReRAM, and simulate them
- Tyler Kloser: Get the ReRAM cell to simulate and create more specific characteristics with the new suggestions from our client
- Austin Miller: Explore a new 1(s)1R (1 Selector, 1 Resistor) structure to see if it can be fabricated with the sky130 process (depending on advisor and client input)
- Vinicius Malaman Soares: Get ReRAM to simulate and work on characterizations according to this week's meeting.

- **Summary of weekly advisor meeting**
  - Unfortunately, our professors (advisor and client) had a late meeting come up during our scheduled time, so we were unable to have a face-to-face meeting this week. We did, however, receive some input from our client on our proposed modules and characterization tests. Dr. Wang likes what we have so far, but had a couple of questions and some additional tests to run and data to collect during the already proposed tests